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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/669,034	09/25/2000	Ganesh Subramaniyam	042390.P9043	3498

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EXAMINER	
PHAN, RAYMOND NGAN	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 11/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/669,034	SUBRAMANIYAM ET AL.	
	Examiner	Art Unit	
	Raymond Phan	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5 and 7-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5 and 7-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Part III DETAILED ACTION

Notice to Applicant(s)

1. This action is responsive to the following communications: amendment and remarks filed on August 31, 2005

2. This application has been examined. Claims 1-3, 5, 7-19 are pending.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-3, 5, 7-19, are rejected under 35 U.S.C. § 103(a) as being unpatentable over Thomas et al. (US No. 5,752,011) in view of Shiell et al. (US NO. 6,138,232).

In regard to claims 1, 8, Thomas et al. disclose a method and system controlling a CPU's clock based on the processor's temperature and activity, wherein the CPU includes programmable logic array 8 (see col. 6, lines 1-34) to operate as an interrupt handler to control CPU upon receiving an interrupt 18 (see figure 3, col. 4, line 64 through col. 5, line 38). But Thomas et al. do not specifically disclose the first quantity of instruction per cycle in first mode and second quantity of instructions per cycle in second mode. However Shiell et al. disclose the first quantity of instruction per cycle in first mode (i.e. partial mode) and second quantity of instructions per cycle in second mode (i.e. full mode) (see col. 9, lines 25-40). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the

teachings of Shiell et al. within the system of Thomas et al. because it would reduce the power consumption in the computer system.

In regard to claims 2, 15, Thomas et al. disclose wherein the power management logic comprising a thermal sensor 4 (see figure 5); and an interrupt generating hardware 16 coupled to the digital filter, wherein the interrupt generating hardware generates a first interrupt whenever the temperature of the CPU exceeds the predetermined threshold and generates a second interrupt whenever the temperature of the CPU is below the predetermined threshold (see figure 3, col. 7, line 51 through col. 8, line 5). The teaching of digital filter is explicitly known to the teaching of Thomas et al. (see col. 5, line 65 through col. 6, line 17).

In regard to claims 3, Thomas et al. disclose an analog to digital converter coupled between the thermal sensor and the digital filter (see figure 9).

In regard to claim 5, 9, 17, Shiell et al. disclose wherein the power management logic further comprises an instruction execution unit coupled to the interrupt handler (see col. 6, lines 4-50); an artificial activity generator coupled to the interrupt handler (see col. 4, lines 7-58). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Shiell et al. within the system of Thomas et al. because it would reduce the power consumption in the computer system.

In regard to claim 11-14, 18, Thomas et al. disclose wherein the CPU to operate in a full dispersal mode whenever the die temperature is below the predetermined threshold temperature and operates in a single dispersal mode whenever the temperature of the CPU is above the predetermined threshold temperature (see col. 14, lines 47-67). But Thomas et al. do not specifically

disclose the instruction execution unit. However Shiell et al. disclose the instruction execution unit executes the numbers of instruction based on the predetermined frequency from the interrupt (see col. 4, lines 7-58). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Shiell et al. within the system of Thomas et al. because it would reduce the power consumption in the computer system.

In regard to claims 7, 10, 19, Thomas et al. disclose wherein the artificial activity generator causes the CPU artificial activity generator to suspend artificial activity within the CPU whenever the die temperature is above the predetermined threshold temperature (see col. 6, lines 35-67).

In regard to claim 16, Thomas et al. disclose a method and system controlling a CPU's clock based on the processor's temperature and activity, wherein the CPU includes programmable logic array 8 (see col. 6, lines 1-34) to operate as an interrupt handler to control CPU upon receiving an interrupt 18 (see figure 3, col. 4, line 64 through col. 5, line 38); the thermal sensor 4 (see figure 5). But Thomas et al. do not specifically disclose the instruction execution unit indicating execution of first quantity of instruction per cycle in first mode and second quantity of instructions per cycle in second mode. However Shiell et al. disclose instruction execution unit indicating the execution of the first quantity of instruction per cycle in first mode (i.e. partial mode) and second quantity of instructions per cycle in second mode (i.e. full mode) (see col. 9, lines 25-40). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Shiell et al.

within the system of Thomas et al. because it would reduce the power consumption in the computer system.

Response to Arguments

7. In view of amendment and remark filed on August 31, 2005, claims 1-3, 5, 7-19 have been fully considered but they are not deemed to be persuasive.

Applicant(s) argue that ...Shiell fails to teach or suggest a CPU to execute a first quantity of instruction per cycle whenever a temperature CPU exceeds a predetermined threshold and to execute a second quantity of instruction per cycle whenever a temperature CPU below a predetermined threshold... (page 14). The Examiner does not agree. Shiell discloses SMM management which enable the CPU to execute number of instructions per cycle for a partial power mode and execute the number of instructions per cycle for full power mode (see table 1, col. 9, line 17-39). For the sake of argument, the more CPU processing (increased number of instructions), the more power it's consumed and the more heat is produced and in contrast, reducing the number of CPU processing, the less power it's consumed and less heat is produced.

Applicants argue that "...changing the clock frequency in order to control the temperature is not equivalent to changing the quantity of instruction executed by the CPU...". Examiner does not agree with this statement. The power management technology for the CPU has been well-known to skilled person in the art that in order to reduce the power consumption of the CPU, one must reduce the clock frequency of the CPU and the heat will be reduced accordingly. Thus the number of instruction per cycle would reduce at the certain reduced clock frequency.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Conclusion

8. Claims 1-3, 5, 7-19 are rejected.

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. § 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. § 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Raymond Phan, whose telephone number is (571) 272-3630. The examiner can normally be reached on Monday-Friday from 6:30AM- 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's Primary, Paul Myers can be reached on (571) 272-3639 or via e-mail addressed to paul.myers@uspto.gov. The fax phone number for this Group is (703) 872-9306.

Communications via Internet e-mail regarding this application, other than those under 35 U.S.C. 132 or which otherwise require a signature, may be used by the applicant and should be addressed to [**raymond.phan@uspto.gov**].

All Internet e-mail communications will be made of record in the application file. PTO employees do not engage in Internet communications where there exists a possibility that sensitive information could be identified or exchanged unless the record includes a properly signed express waiver of the confidentiality requirements of 35 U.S.C. 122. This is more clearly set forth in the Interim Internet Usage Policy published in the Official Gazette of the Patent and Trademark on February 25, 1997 at 1195 OG 89.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see hop://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 central telephone number is (571) 272-2100.

Raymond Phan
November 9, 2005

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
11/14/05